DS_DMA - Development # 48: AMBPEX5_SX50T_WISHBONE

Status:	Confirmed	**Priority:**	Normal
Author:	Dmitry Smekhov	**Category:**	
Created:	04/20/2013	**Assignee:**	Dmitry Smekhov
Updated:	07/01/2013	**Due date:**	07/01/2013
Subject:	AMBPEX5_SX50T_WISHBONE		
Description:	PCI Express controller for WISHBONE bus; Virtex5 SX50T PCI Express v1.1 x8		

History

04/21/2013 01:26 am - Dmitry Smekhov

Simulation is ok. Revision r17

05/12/2013 04:06 am - Dmitry Smekhov

Correct core64_pb_disp; Add signals *timeout_cnt*, *slave_timeout*

06/23/2013 10:45 pm - Dmitry Smekhov

Add register in the TEST_GEN block:

0x10 - STATUS

0x11 - BLOCK_WR

0x12 - sig 0xAAAAAAAAA - is temporary word

wb_test read data from TEST_GEN with errors.

Revision: r30

07/01/2013 02:09 am - Dmitry Smekhov

I set 125 MHz to clk for WISHBONE bus.

Data transfered from TEST_GEN to computer without error.

Revision r32