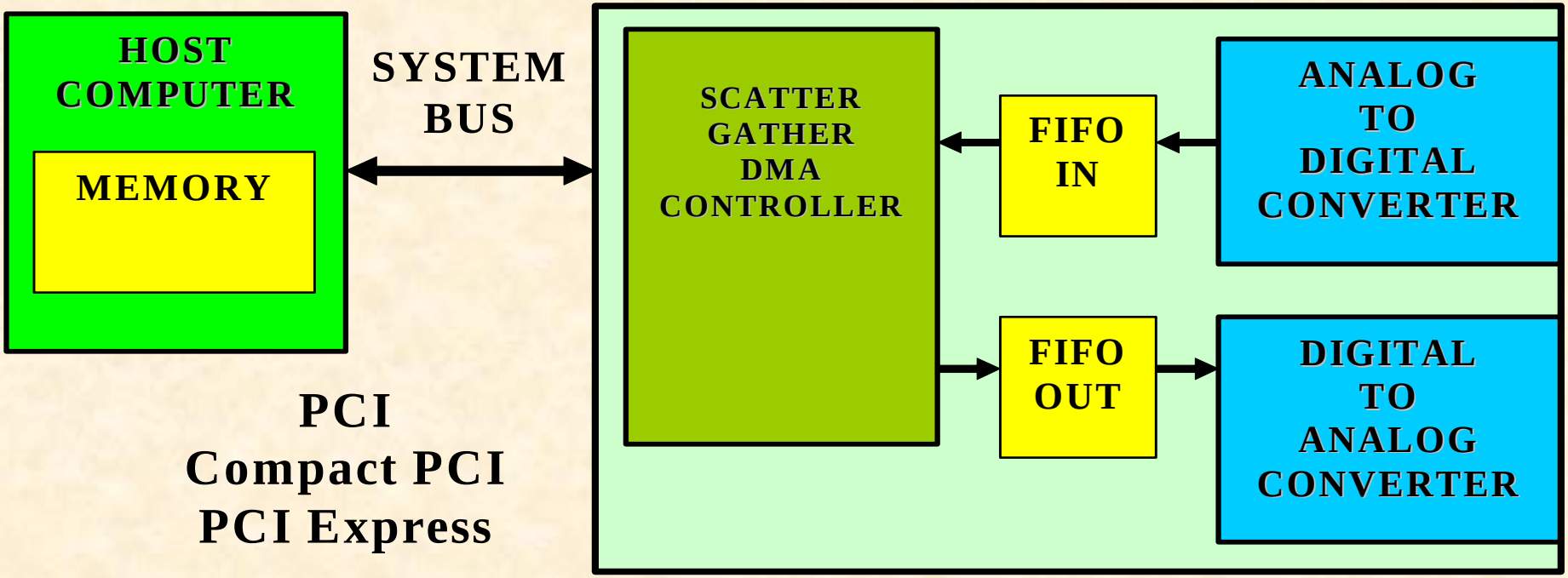
Scatter-Gather DMA IP CORE for PLDA EZDMA IP

Dmitry Smekhov

Instrumental Systems Corp.

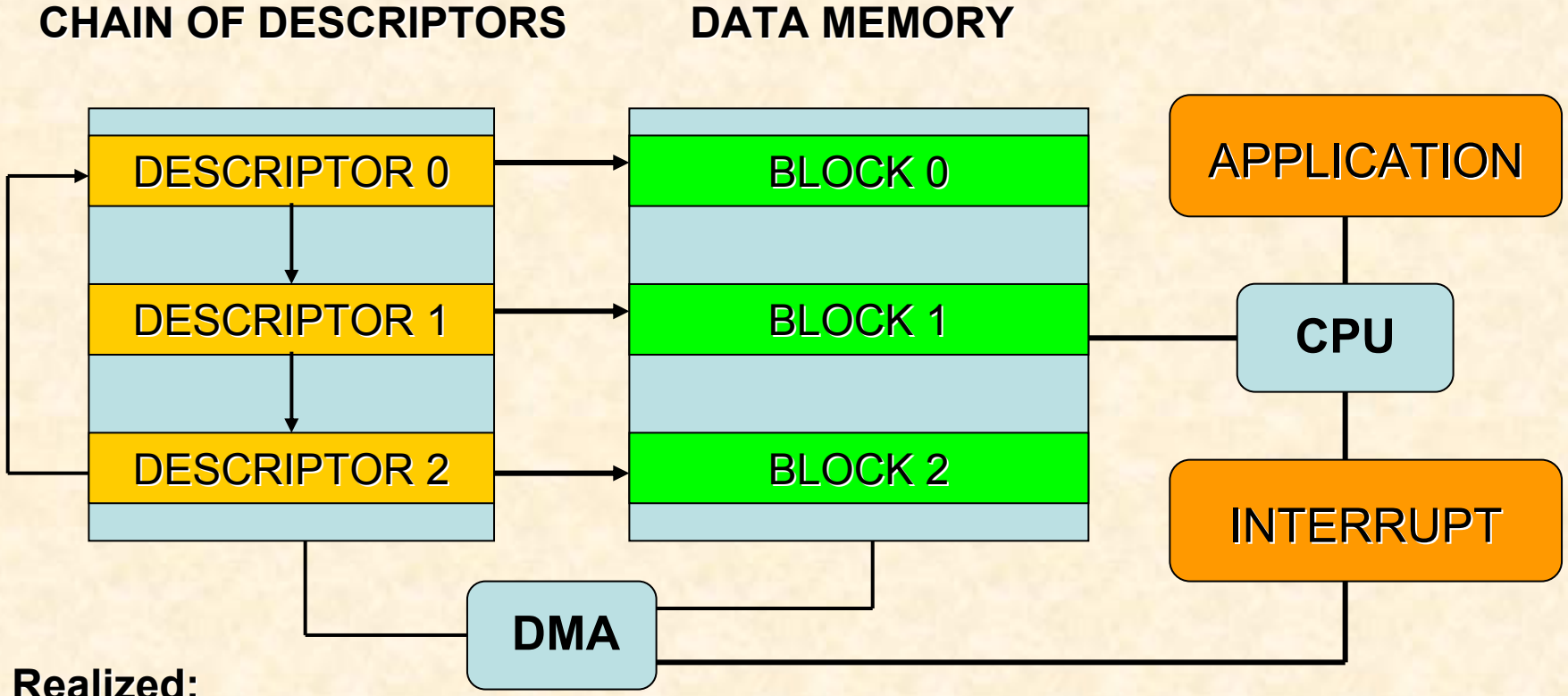
Moscow, Russia

TYPICAL SYSTEM



PCI
Compact PCI
PCI Express

SCATTER-GATHER MODE



Realized:

1. **PCI9056, PEX8311 from PLX Technology**
2. **EZDMA from PLDA**
3. **IP Core from Nortwest Logic**

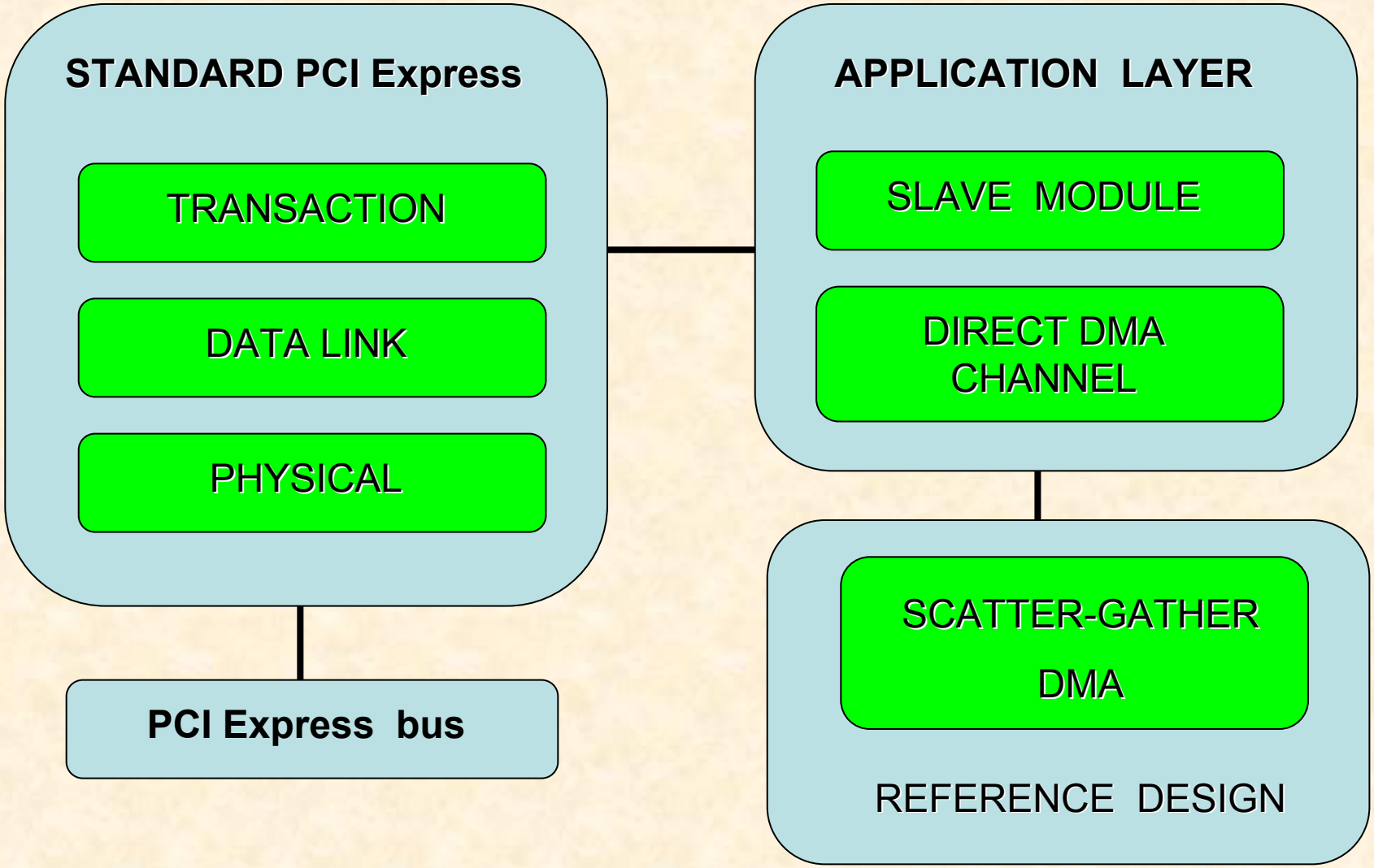
ATTENTION !!!

DATA BLOCK IS CONTINUOUS PHYSICAL ADDRESES

PCI Express solution

- LogiCORE Endpoint from Xilinx
- DesignWare from Synopsys
- EZDMA from PLD Application

EZDMA IP


STANDARD PCI Express
TRANSACTION
DATA LINK
PHYSICAL
PCI Express bus
APPLICATION LAYER
SLAVE MODULE
DIRECT DMA CHANNEL
SCATTER-GATHER DMA
REFERENCE DESIGN

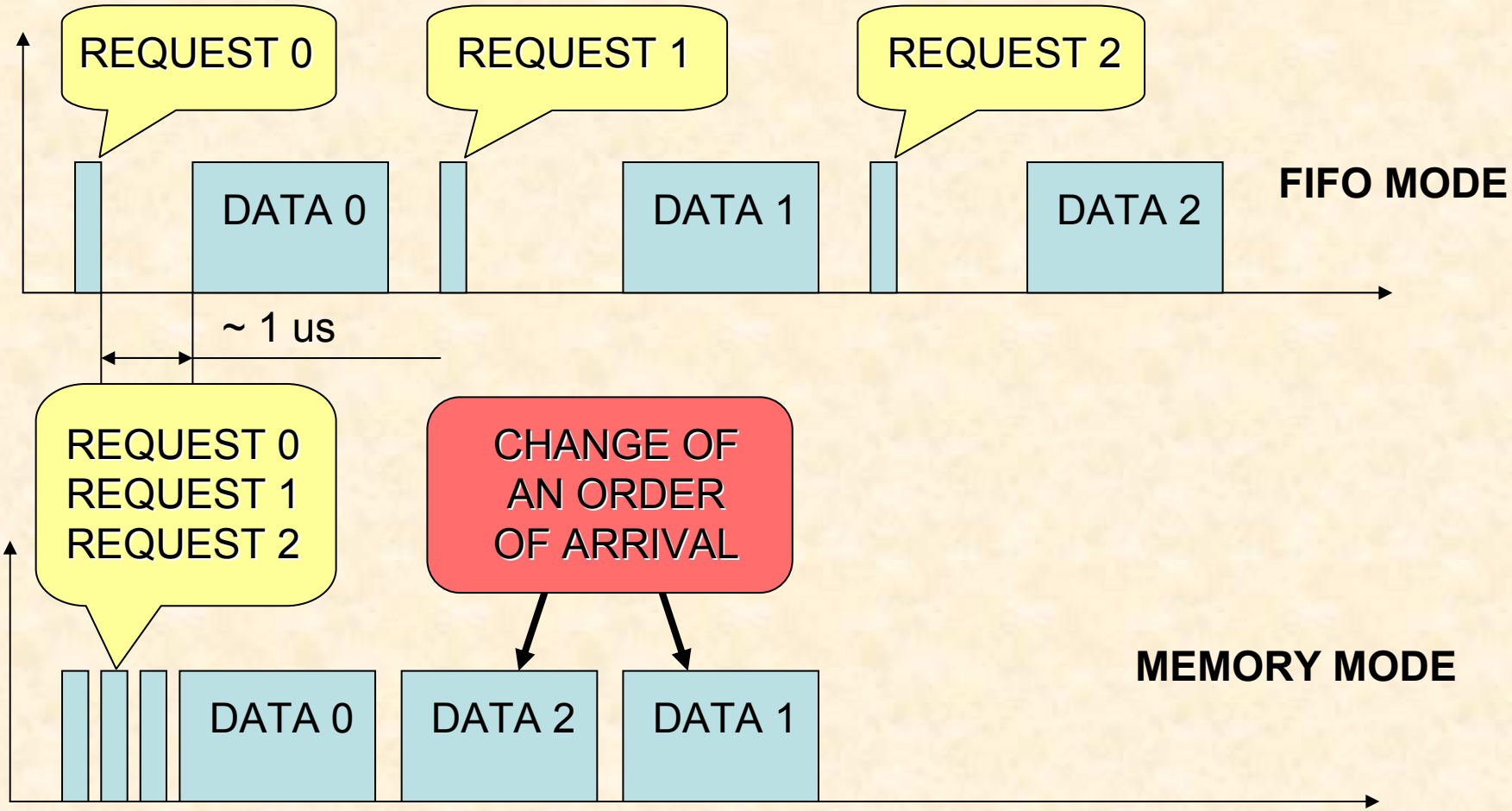
EXISTING PROBLEMS

During operations with EZDMA IP Core
there are several problems:

- **THE LOW SPEED DURING THE DATA TRANSFER FROM THE COMTUTER TO A DEVICE IN FIFO MODE**
- **A “COMPLETION TIMEOUT” ERROR**
- **THE LOW SPEED OF WORKING WITH FRAGMENT MEMORY**

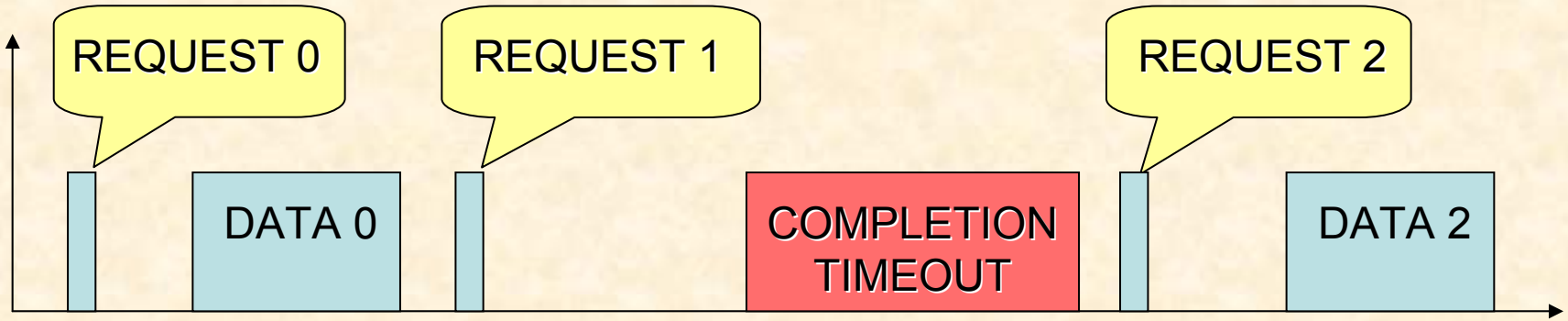
FIRST PROBLEM

- **THE LOW SPEED DURING THE DATA TRANSFER FROM THE COMTUTER TO A DEVICE IN FIFO MODE**



SECOND PROBLEM

- **THE COMPLETION TIMEOUT ERROR**



DATA 1 IS LOSS

THE DMA CHANNEL ONLY INFORMS ABOUT THE COMPLETION TIMEOUT ERROR, BUT DOESN'T CORRECT IT

P965, P45 chipset – 1 error per 4 hour

THIRD PROBLEM

- THE LOW SPEED OF WORKING DURING TRANSFER ON FRAGMENT MEMORY

TWO WAYS OF MEMORY ALLOCATION

SYSTEM MEMORY

- CONTINUOUS PHYSICAL AND VIRTUAL ADDRESSES
- SMALL SIZE
- 128 Mbytes
- 32 blocks of 4 MB

DMA read out descriptor for each block of 4 MB

USER MEMORY

- CONTINUOUS VIRTUAL ADDRESSES ONLY
- SEPARATED ON 4kB PAGE
- BIG SIZE
- 1536 Mbytes
- 32 blocks of 48 MB
- 12288 pages on block

DMA read out descriptor for each 4kB page

MAIN FEATURES

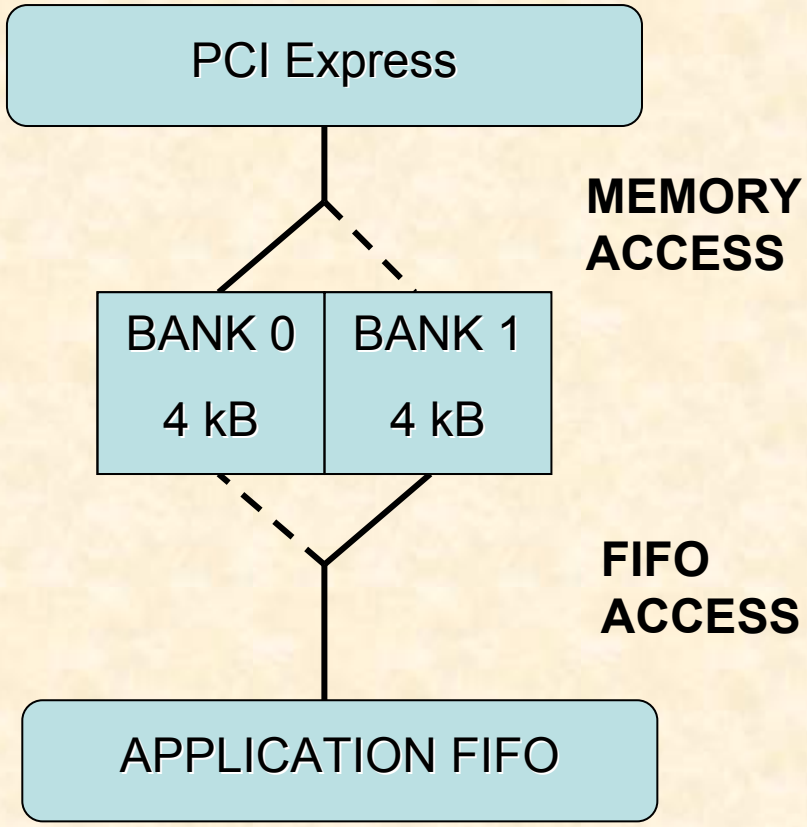
Separate descriptors have been united in the special block of descriptors

0	SIZE0	ADR0
1	SIZE1	ADR1
2	SIZE2	ADR2
…		
62	SIZE62	ADR62
63	CRC / SIG	NEXT

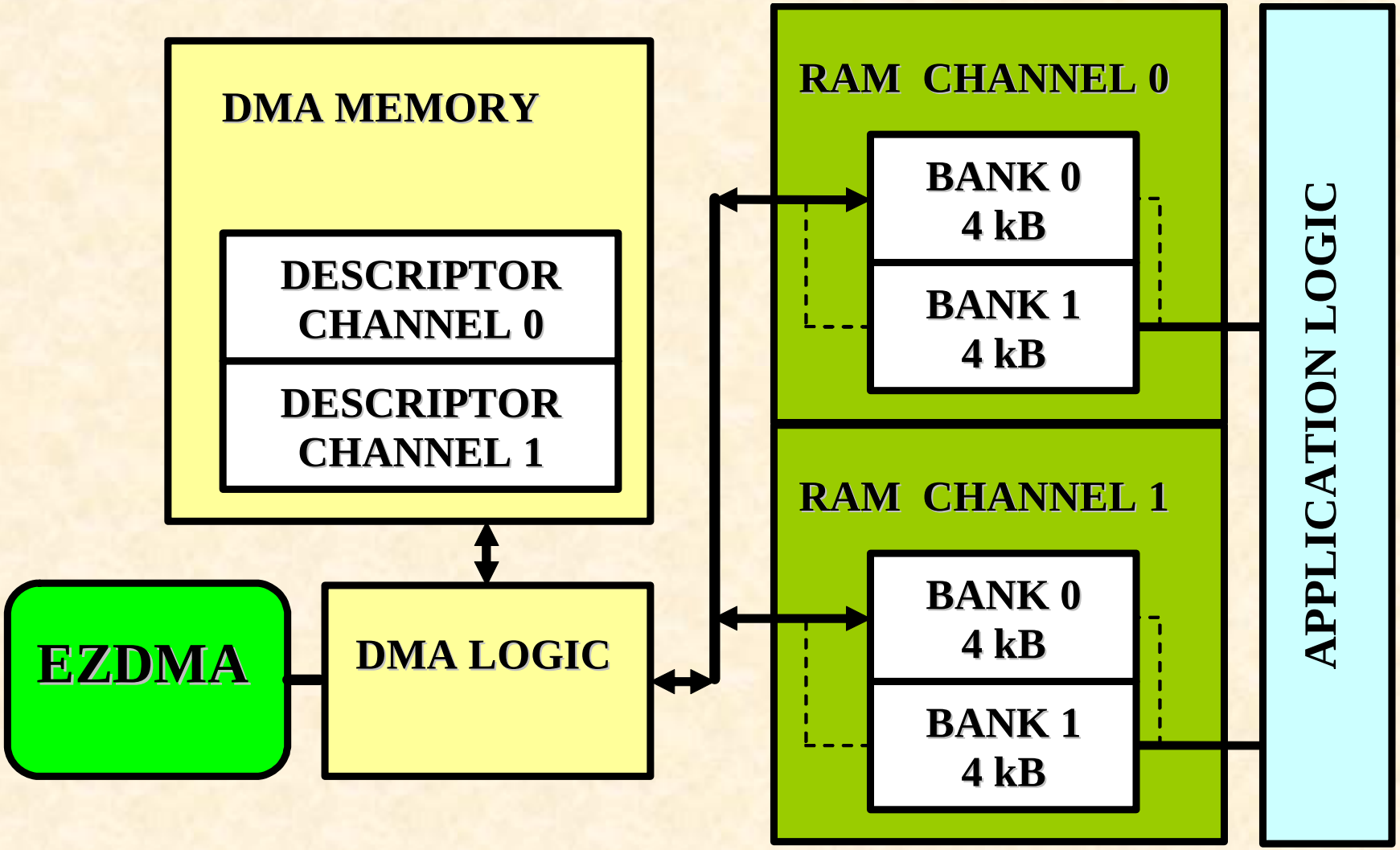
Block size is 512 bytes

CRC and SIG protect the system from a mistake in the descriptors block

There is a special block of dual-bank and dual-port memory



NEW CONTROLLER



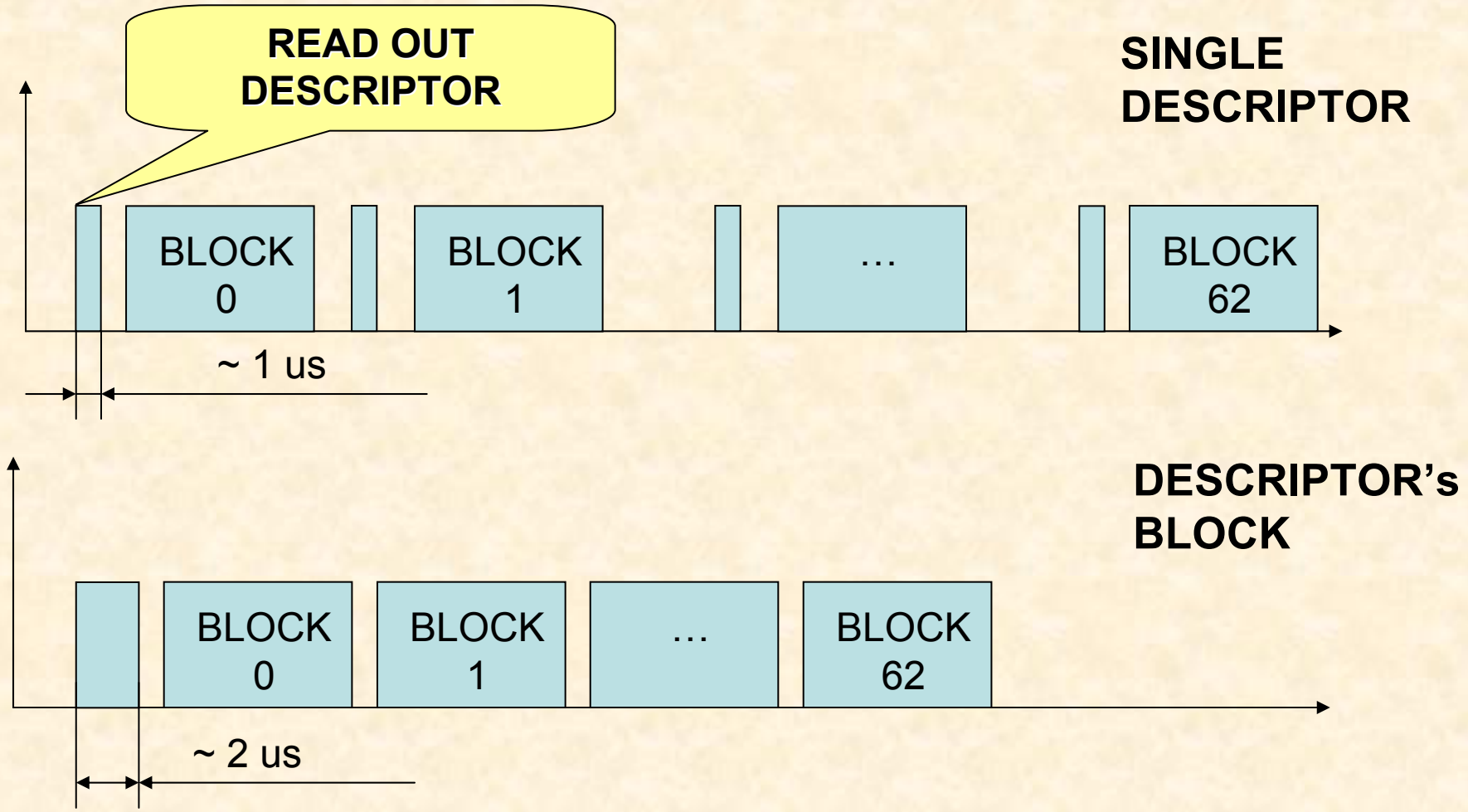
RESOLVING OF PROBLEMS

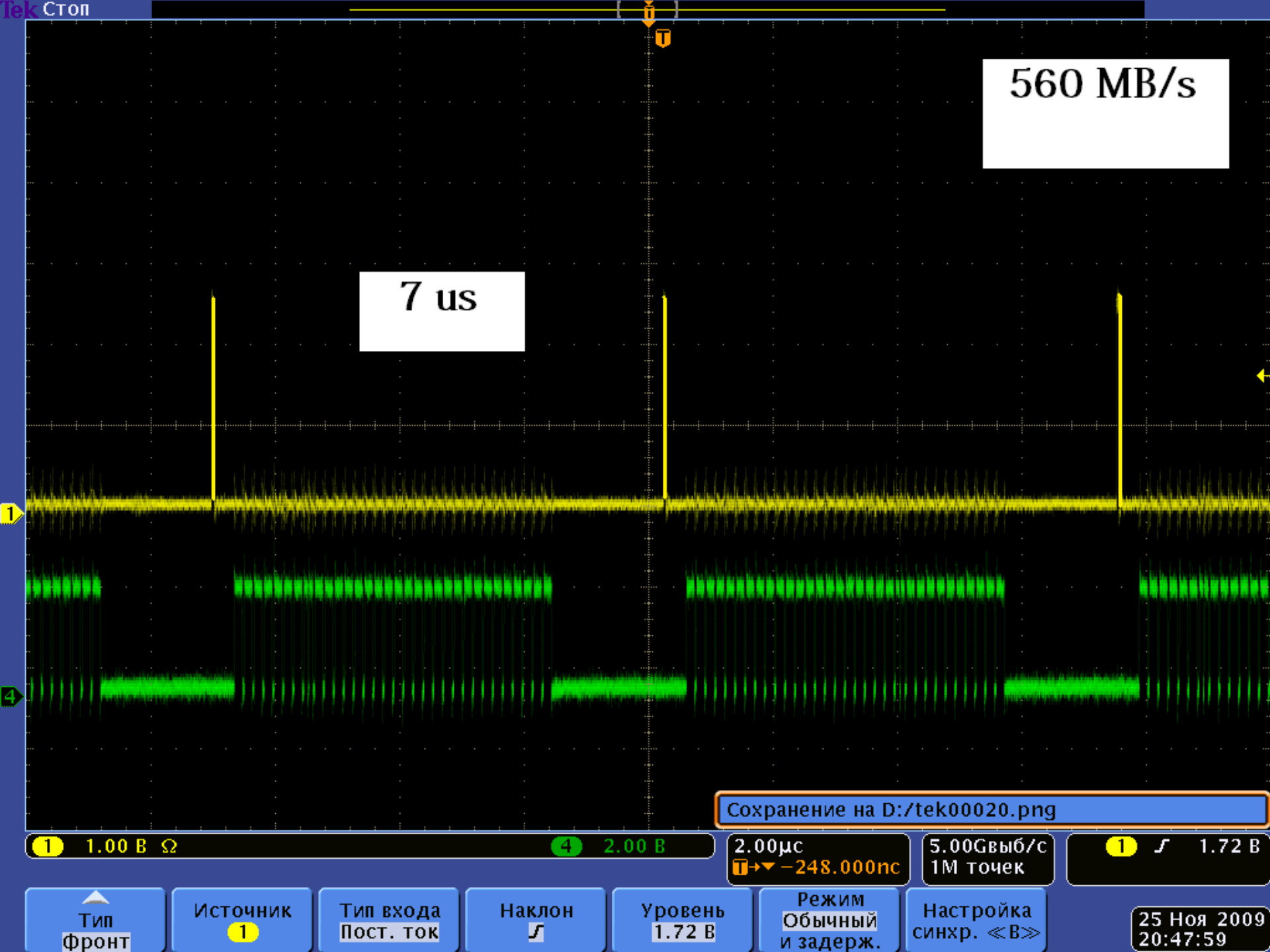
The DUAL BANK MEMORY resolves the first and the second problems:

1. The DMA Controller sends several read requests providing the maximum speed of data read out. Answers can come in any order. They are registered in the memory bank according to their address.
2. In the case of a occurrence of the “Completion Timeout” error the repeated cycle of filling the memory bank starts.

RESOLVING OF PROBLEMS

- The DESCRIPTOR's BLOCK resolves the third problem




Tek Стоп
560 MB/s
7 us
Сохранение на D:/tek00020.png
1 1.00 В Ω
4 2.00 В
2.00µс
T→▼ −248.000nc
5.00Gвыб/с
1M точек
1 1.72 В
Тип
Фронт
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1
Тип входа
Пост. ток
Наклон
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Режим
Обычный
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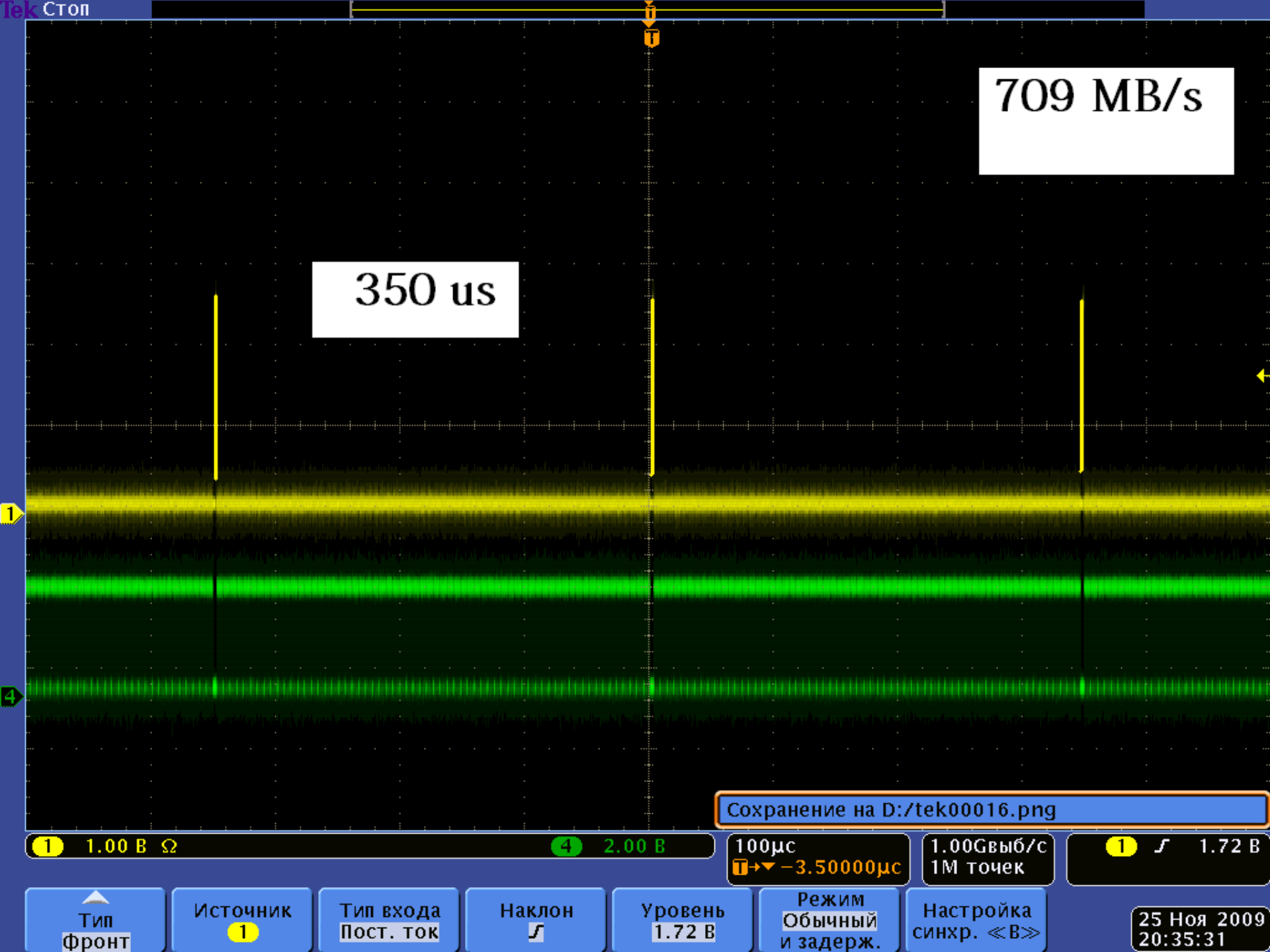
Tek Стоп
709 MB/s
350 us
Сохранение на D:/tek00016.png
1 1.00 В Ω
4 2.00 В
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Режим
Обычный
и задерж.
Настройка
синхр. ≪В≫
25 Ноя 2009
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RELEASES

AMBPEX8

Virtex 4 XC4VFX20

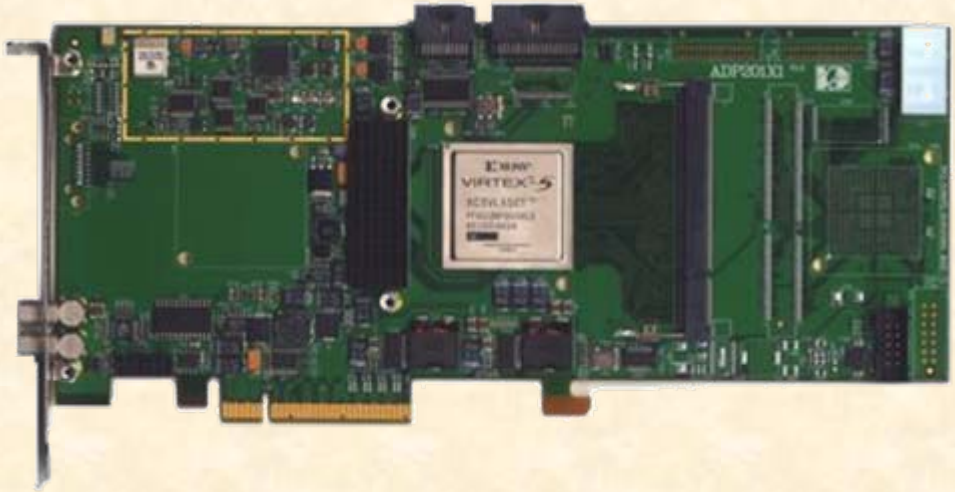
PCI Express x4

DUAL FPGA:

XC4VFX20 – PCIE Controller

XC4VSX35 – APPLICATION

ADP201x1



Virtex 5 XC5VLX50

PCI Express x8

SINGLE FPGA :

APPLICATION and

PCIE Controller

RESULTS

MODULE	INPUT FROM DEVICE		OUTPUT TO DEVICE	
	SYSTEM 128 MB	USER 1536 MB	SYSTEM 128 MB	USER 1536 MB
ADP201x1 Virtex 5 PCIE x8 INTEL P55	**1535** MB/s	**1522** MB/s	**1077** MB/s	**1069** MB/s
			UNSTABLE	
ADP201x1 Virtex 5 PCIE x8 INTEL P45	**1440** MB/s	**1420** MB/s	**730** MB/s	**712** MB/s
AMBPEX8 Virtex 4 PCIE x4 INTEL P45	**714** MB/s	**709** MB/s	**521** MB/s	**518** MB/s

COMPARISONS

MODULE	INPUT FROM DEVICE		OUTPUT TO DEVICE	
	SYSTEM	USER	SYSTEM 128 MB	USER 1536 MB
ADP201x1	**1534** MB/s	**1522** MB/s	**1089** MB/s	**1086** MB/s
NVIDIA GeForce 8800	**1643** MB/s	**1273** MB/s	**1558** MB/s	**1299** MB/s

ASUSTEK P5N-E SLI PCI Express 1.1 x8

CONCLUSIONS

The new Scatter-Gather DMA component have been developed. This DMA component provides the next possibilities:

1. Fast work with the fragment memory.

2. Correction of the “Completion Timeout” error.

3. Fast data transfers to a device in the FIFO mode.

CONTACTS

Instrumental Systems Corp.

Moscow, Russia

Dmitry Smekhov

WWW: http://www.insys.ru

E-mail: dsmv@insys.ru

Skype: dsmekhov

Thank you for your attention!